WAQAS NASIR

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SUMMARY

Early career Electrical Engineer with experience in FPGA design and verification, including RTL development using Verilog and SystemVerilog for digital systems. Familiar with FSM design, synchronous logic, FIFO design, and timing analysis, along with exposure to SystemVerilog testbenches and UVM-based environments. Knowledge of structured verification approaches including test planning, assertions, constrained-random testing, and functional coverage. Experienced in simulation, waveform debugging, and analyzing system behavior under normal and fault conditions, with basic Python scripting for automation workflows.

TECHNICAL SKILLS

Verification: SystemVerilog, UVM concepts, assertions (SVA), constrained-random testing, functional coverage.
Test Engineering: Test plan exposure, requirement traceability, validation workflows, failure analysis.
Simulation & Debug: ModelSim / QuestaSim, waveform analysis, protocol validation, debugging.
RTL Understanding: Verilog, CDC, pipelining, RTL design, FSM design, synchronous logic, timing analysis.
Automation: Python scripting for regression execution, log parsing, and result reporting.
Tools: Xilinx Vivado, ModelSim/QuestaSim, Oscilloscope, Logic Analyzer, Digital Multimeter.

WORK EXPERIENCE

The Boeing Company — Saint Louis, MO
Systems Engineer — *July 2023 - June 2024*

- Implemented ModelSim regressions using Python scripts, observing coverage tracking and reduced manual effort.
- Practiced FSM and FIFO RTL verification using UVM with SystemVerilog, understanding state transitions and data flow.
- Gained exposure to PCB layout design, component placement and signal routing across printed circuit board designs.
- Worked on design reliability improvements through waveform analysis and assertions to identify edge-case failures.

INTERNSHIPS

NASA — Orlando, FL
Intern — *Aug 2022 - Dec 2022*

- Using Verilog, developed RTL modules to implement FSM logic and ensure correct functionality across design conditions.
- Through Vivado tools, supported FPGA synthesis and analyzed timing across configurations, building timing awareness.
- By designing digital logic, contributed to FIFO and control modules and supported proper data flow across systems.
- Using hardware concepts, assisted in integrating RTL modules and verifying signal interactions across modules.

Samsung — New York City, NY
Intern — *Jan 2022 - May 2022*

- Through Python scripting, contributed to expanding edge-case coverage by simulating concurrent read/write scenarios.
- Using SystemVerilog and UVM concepts, supported FIFO validation and observed pointer synchronization behavior.
- By applying assertions and waveform debugging, it helped identify faults and understand system behavior.
- With simulation tools, assisted in evaluating control logic under concurrent and stress test conditions.

PROJECTS

New York, NY
May 2024 – Present

FIFO Verification Testbench

- Designed testbench components to verify FIFO behavior and debug data mismatches / ordering.

FSM and Control Logic Design

- Developed RTL for FSM and control logic to implement state transitions and manage signal flow across design states.

Regression and Automation Framework

- Created Python workflows to run regression tests and analyze failures across simulation scenarios.

EDUCATION

City University of New York - College of Staten Island - B.S. Electrical Engineering (ABET) - May 2023