Jonathan Pierre-Louis

347-679-5407 | jonathan.pierrelouis23@gmail.com | linkedin.com/in/jonathanpl23 | github.com/ScorageLEL

Summary

Computer Engineering graduate with hands-on experience in DRAM verification, SPICE simulation, hardware validation, and test automation. Proficient in Python, MATLAB, Verilog, and industry EDA tools including LTspice. Proven ability to deliver technical results and communicate complex concepts effectively in collaborative team environments.

Education

The City College of New York - New York, NY May 2026
Bachelor of Engineering in Computer Engineering *GPA: 3.2*

Experience

Development Command Army Research Laboratory (DEVCOM ARL) Adelphi, MD
HBCU/MI Summer Research Intern *June 2025 – August 2025*

- Performed **hardware validation** and **device characterization** of ultra-wide band-gap semiconductor devices using **test equipment**, analyzing electrical behavior to validate performance specifications and ensure design requirements were met
- Configured **Zurich Instruments MFIA Impedance Analyzer** and developed **MATLAB** scripts to automate data collection and **circuit analysis**, identifying performance trends and troubleshooting device issues through **systematic debug** methodologies
- Authored **test procedures** and **validation documentation** detailing characterization methodologies, collaborating with **cross-functional teams** to enable knowledge transfer and establish **best-known methods** for hardware validation

Micron Atlanta, GA
DRAM Design Verification Engineering Intern *June 2023 – August 2023*

- Developed **Python** automation infrastructure to perform **timing analysis** and **functional verification** across thousands of DRAM simulations, implementing **verification methodology** to identify timing violations and improve **test coverage** and **design quality**
- Engineered data visualization and **coverage analysis** tools using **matplotlib** to track **functional coverage** metrics and identify design bugs, supporting **coverage-driven verification** methodology and enabling **systematic debugging** across DRAM product architectures
- Built **automated regression testing** and **continuous integration** infrastructure using **Python scripting**, improving **verification workflow** efficiency and enabling rapid iteration on design improvements across multiple DRAM configurations

Braverhood New York, NY
Community Habilitation Worker *January 2022 – Present*

- Delivered individualized support to individuals on the autism spectrum, adapting **communication** approaches to explain complex concepts and developing customized solutions, while collaborating with families to implement action plans and achieve client objectives

Projects

4-Bit Ripple Carry Adder | Digital Integrated Circuits Course April 2025 – May 2025

- Designed and **verified** a 4-bit full adder at transistor level using 144 **CMOS transistors**, performing **SPICE simulations** with **LTspice** to verify circuit functionality, **timing characteristics**, and validate logic operation across process corners
- Constructed complete **circuit layout** using **Electric VLSI EDA** tool, extracted **layout parasitics**, and performed **post-layout simulations** to ensure timing closure, then executed **Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification** to confirm design integrity
- Analyzed circuit performance including **propagation delay, power consumption, and noise margins** across multiple voltage and temperature conditions, demonstrating understanding of **CMOS circuit behavior** and optimization techniques for digital circuit design

Leadership Experience

Vice President, National Society of Black Engineers (NSBE) CCNY Chapter July 2025 – June 2026

- Led **cross-functional partnerships** with corporate sponsors and university departments, establishing strong stakeholder relationships to expand professional development opportunities for 50+ chapter members

President, Society of Hispanic Professional Engineers (SHPE) CCNY Chapter May 2024 – June 2025

- Spearheaded strategic outreach to industry partners that doubled annual chapter programming from 16 to 30+ events, managed a 5-person executive board, and demonstrated **initiative** and **time management** skills